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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/612,033

07/03/2003

Tadashi Iguchi

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01/06/2009

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EXAMINER

QUINTO, KEVIN V

ART UNIT

PAPER NUMBER

2826

MAIL DATE

DELIVERY MODE

01/06/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/612,033	Applicant(s) IGUCHI ET AL.	
	Examiner Kevin Quinto	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 September 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4,5,7-11 and 14-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4,5,7-11,14-16,18,19,21 and 22 is/are allowed.
- 6) ☒ Claim(s) 17 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. This Office action is in response to the Request for Continued Examination under 37 CFR 1.114 filed on September 29, 2008.

Response to Arguments

2. The examiner notes newly amended claim 17 and thus hereby withdraws the objection made to claims 17 and 20 in the previous Office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kinoshita (United States Patent Application Publication No. US 2002/0179962 A1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

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either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

5. In reference to claim 17, Kinoshita (United States Patent Application Publication No. US 2002/0179962 A1) discloses a method which meets the claim. Figures 4-28 and 34-57 each discloses a method of manufacturing a semiconductor memory which comprises making floating gate electrodes (26, 43, 58) on a semiconductor substrate (5) at memory cell forming regions. The floating gate electrodes (26, 43, 58) have a predetermined gate width. A plurality of first trenches is formed in the semiconductor substrate (5). Each first trench is made between adjacent ones of the floating gate electrodes (26) along a gate width direction. The first trenches are in self-alignment to the floating gate electrodes (26). Element isolating regions (24) are made by filling isolating fillers in the first trenches. A side wall spacer (30, 62) is formed on a surface of each of the isolating fillers (24) on a side wall of the floating gate electrodes (26, 43, 58). The side wall spacer (30, 62) is in self-alignment to the floating gate electrodes (26, 43, 58). A plurality of second trenches is made in the isolating fillers filled in the first trenches using the side wall spacer (30, 62) as a mask. The second trenches have a narrower width at a bottom thereof than at a top. The maximum width of the second trenches is smaller than a width of the first trenches. A word line (11, 46) extending along the gate width direction is formed in the second trenches.

6. In reference to claim 20, each of the second trenches has a second gate insulating film (10, 45) formed on its inner surfaces.

Allowable Subject Matter

7. Claims 5, 15, and 22 are allowed. Claims 4, 7-11, 14, 16, 18, 19 and 21 were allowed in a previous Office action.

8. The following is an examiner's statement of reasons for indicating allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a semiconductor memory or its method of fabrication with each memory cell having a floating electrode and a wordline embedded within a trench that is itself formed within a trench insulation structure between adjacent memory cells having the explicit trench structure as described in claims 5 and 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin Quinto/
Examiner, Art Unit 2826

/Evan Pert/
Primary Examiner, Art Unit 2826